14. (Amended) A lead frame for an integrated circuit chip having a frame engaging bottom surface comprising:

an apertured frame said frame being generally circular and defining a peripheral edge and having a contact surface for securing the chip thereto, said edge being disposed within an outer chip edge for minimizing fillet formation.

Please add claim 15 as follows:

--15. The lead frame of claim 1, wherein said chip-supporting surface engages the bottom of the chip at a location remote from higher stress regions associated with the chip.--

REMARKS

Claim 15 is added. Claims 1, 2, 6, 8, 9, 13 and 14 are amended. The attached "VERSION WITH MARKINGS TO SHOW CHANGES MADE" shows changes made to the amended claims with deletions bracketed and additions underscored. Claims 1-15 are pending in the Application.

A. DRAWING OBJECTIONS

Figs. 6, 6A and 6B are objected to because "they should be designated by a legend such as --Prior Art--." Applicants file herewith a separate Request for Approval of Drawing Corrections which includes amendments to Figs. 6, 6A and 6B.

The drawings are objected to because "references signs 55, 63 and 88 are not shown." Applicants file herewith a separate Request for Approval of Drawing Corrections which includes amendments to Fig. 1A. Applicants respectfully traverse this objection with respect to reference sign 88.

Fig. 3 shows reference sign 88.

Applicants respectfully request withdrawal of the objection to the drawings on this ground.

B. THE 35 U.S.C. §112 CLAIM REJECTIONS

Claim 2 is rejected, under 35 U.S.C. §112, ¶2, because "claim 2 recites the phrase 'high stress regions' . . . [which] implies a comparison between regions without previously quantity." Claim 2 is amended so that claim 2 recites "higher stress" rather than "high stress."

Claims 1-11 and 13 are rejected, under 35 U.S.C. §112, ¶2, because claim 1 recites "the corresponding;" claim 2 recites "the high," "the corners" and "the risk;" claim 6 recites "said respective:" claim 9 recites "said connections," "said respective" and "the vicinity;" and claim 13 recites "the side chip" and "the lower surface." Claims 1, 2, 6, 9 and 13, from which claims 3-5, 7, 8, 10, 11 and 13 depend, are amended.

Claims 1 and 2 (the last cited occurrence of "the") are amended to change "the" to "a." Claim 2 is amended to delete the first cited occurrence of "the" and change "the high" to "higher." Claim 6 is amended to delete the cited occurrence of "respective." Claim 8 is amended similarly. Claim 9 is amended to change "said" to "a."

Claim 13 is amended to change "side" to "circuit" and "lower" to "bottom." Support for the former amendment is contextual and also found in the specification at page 5, lines 14-17. Support for the latter amendment also is contextual.

The foregoing Amendments are for clarity and not overcoming prior art.

Applicants traverse the rejection as to "the vicinity" in claim 9. "The vicinity" is an English-language colloquialism comparable to "near" or "around." The phrase does not refer to a specific element, rather a relative orientation.

Applicants respectfully request withdrawal of the rejection of claim 9 on this ground.

C. THE 35 U.S.C. §102 AND §103 CLAIM REJECTIONS

Claims 1-3 and 6-13 are rejected, under 35 U.S.C. §102(b), as being anticipated by Chun. Claims 4 and 5 are rejected, under 35 U.S.C. §103(a), as being unpatentable over Chun, in view of Djennes *et al.* or Yoo, respectively. Applicants respectfully traverse these rejections.

Under 35 U.S.C. §102, a reference must teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present.

Under 35 U.S.C. §103, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in a reference itself or in knowledge generally available to one of ordinary skill in the art, to modify a reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, a prior art reference, or references when combined, must teach or suggest all the claim limitations. The

teaching or suggestion to make the claimed combination and the reasonable expectation of success must be found in the prior art, and not based on Applicants' disclosure.

The invention of claims 1, 12 and 13 is a lead frame. Although "lead frame" occurs only in the preambles of each of claims 1, 12 and 13, each "claim cannot be read independently of the preamble and the preamble must be read to give meaning to the claim or is essential to point out the invention."[1]

It is known to a skilled person in the field of semiconductor device packaging to which the present invention relates, that the term "lead frame" refers to a stamped or etched metal frame that provides external electrical connections for a packaged electrical device.

In contrast to the invention recited in claims 1, 12 and 13, Chun describes a charge coupled device (CCD) package 12 with a glass lid 14 and an insulating tape 15 interposed therebetween. Throughout the full specification and drawings of this document, item 15, shown in Figure 3A, as quoted by the Examiner, is described as an insulating tape, rather than a lead frame. Definitions and disclosures with respect to this item are given at: (a)lines 10 -11, column 3, "an insulation tape"; (b) line 22, column 3, "the insulating tape"; (c) line 27, column 3, "bonding a double-faced insulating tape"; (d) lines 38 - 42, column 4, "A window frame-shaped and double faced insulating tape 15, having a predetermined thickness and a predetermined width, is bonded to the inside of the plurality of conductive bumps 11 on the charge coupled device 12"; (e) lines 49 - 52, column 4, "The glass lid 14 is provided at opposite sides of its lower surface with the plurality of metal lines 13 and is bonded to the upper surface of the insulating tape 15."; (f) lines 7 - 11, column 5, "The insulating tape 15 is adapted for spacing the glass lid 14 from the CCD 12 by a predetermined interval and uses a window frame-shaped tape which is sized to cover neither the conductive bumps 11 of the CCD 12 nor the metal lines 13 of the glass lid 14."; (g) lines 30 - 33, column 5, "The doublefaced insulating tape 15, having the predetermined thickness and the predetermined width, is bonded to the inside of the bond pads 12 of each of the divided CCDs 12."; and (h) lines 41 - 44, column 5, "The glass lid 14 is in turn bonded to the upper surface of the insulating tape 15 on the CCD 12 such that there is provided a predetermined space between the glass lid 14 and the light reception part 12a of the CCD 12."

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[1]Porter v. Farmers Supply Service, Inc. 229 USPQ 814, 816 (Fed. Cir. 1986).

A difference between the claimed invention and Chun is that the present invention provides a crack-resistant integrated circuit package having minimal attachment surface between a semi-conductor chip and a lead frame which limits propagation of cracks and increases the available bonding surface below the chip and encapsulant, whereas Chun provides insulating tape for "providing a predetermined space between the glass lid 14 and the light reception part 12a of the CCD 2".

The significance of the difference highlighted above is that the present invention provides for reliable electrical communication between the integrated circuit chip and the lead frame, whereas Chun provides spacing between CCD elements.

The Office Action asserts that "Chun discloses a lead frame with sidebars 15 . . . having an upper surface for engaging the chip with a *ground ring 13* and leads 19 . . ." (italics added). However, according to the disclosures, in particular item (f) above, *metal lines 13* is not related to insulating tape 15, neither being electrically nor physically in contact. No electrical signals pass between insulation ring 15 and metal lines 13, as would pass between the claimed lead frame and an integrated semi-conductor chip.

In Chun, outlead 19 also is not related to the insulating tape 15. Outlead 19 is "adapted for signal communication and connected to an outer end of each of the metal lines 13 of the glass lid 14." (6:8-10). No electrical signals pass between insulation ring 15 and outlead 19, as would pass between the claimed lead frame and an integrated semi-conductor chip.

Accordingly, insulating tape 15, metal lines 13 and outlead 19 do not teach the lead frame of claims 1, 12 and 13.

Neither Djennas *et al.* nor Yoo *et al.* remedy the deficiencies of Chun with respect to claims 1, 12 and 13.

It is believed that Chun is irrelevant to the claimed invention. Accordingly, no part thereof can be combined with Djennas *et al.* or Yoo *et al.* to suggest or imply that a skilled person derived the claimed device without any inventive exercise.

Chun does not teach every aspect of claims 1, 12 and 13; therefore, claims 1, 12 and 13, and dependent claims 2-3 and 6-11, are allowable over Chun, Djennas *et al.* and Yoo *et al.*

Claim 14 is rejected, under 35 U.S.C. §102(b), as being anticipated by Djennas *et al.* Claim 14 is amended for clarity and not for overcoming prior art. Djennas *et al.* does not anticipate amended claim 14.

The invention of amended claim 14 is a lead frame "being generally circular and defining a peripheral edge . . . disposed within an outer chip edge . . ."

In contrast to the invention of amended claim 14, Djennas *et al.* describes a semiconductor device having window-frame flag 36 with a tapered edge in an opening. Fig. 5 shows a window-frame flag 52 having outer edges 55 extending beyond the edges of the chip 57.

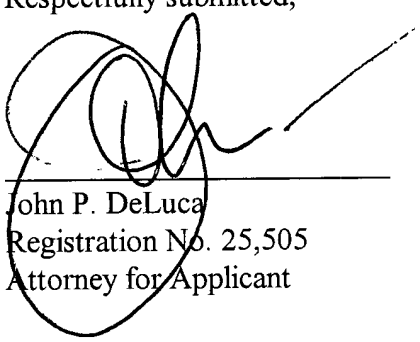
A difference between the invention of claim 14 and Djennas *et al.* is that the present lead frame does not extend beyond edges of a semi-conductor chip, whereas the Djennas *et al.* window-frame flag 52 extends beyond the edges of the chip 57.

The significance of the difference highlighted above is that the invention of claim 14 minimizes fillet formation. Applicants submit herewith a copy of "Achieving Crack Free Package Through Elimination of Type II Failure," by T.C. Chai et al., published September 1999, which discusses other advantages of the invention.

Djennas *et al.* does not teach every aspect of claim 14, therefore claim 14 is allowable over Djennas *et al.*

Applicants respectfully submit that this Application is in condition for allowance. If such is not the case, Applicants invite the Examiner to contact the undersigned to resolve remaining issues.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) A lead frame, for an integrated circuit chip having a frame engaging bottom surface, comprising:

a plurality of sidebars,

each of said sidebars having an inner side and an outer side,

said inner sides defining an aperture,

said outer sides defining a chip-support zone,

said zone being smaller in each dimension than [the] a corresponding dimension of the chip,

each sidebar having an upper chip-supporting surface for engaging the bottom surface of the chip.

2. (Amended) The lead frame of claim 1, wherein said chip-supporting surface engages the bottom of the chip at a location remote from [the high] higher stress regions associated with [the] corners of the chip [to minimize the risk of delamination].

6. (Amended) The lead frame of claim 1, further comprising:

a plurality of support members having proximal and distal ends, each support member being connected to at least one sidebar by said [respective] proximal end thereof.

8. (Amended) The lead frame of claim 7, further comprising:

a plurality of support members having proximal and distal ends, each support member being connected to at least one sidebar by said [respective] proximal end thereof, defining a connection.

9. (Amended) The lead frame of claim 8, wherein each of said connections between each support member and the at least one sidebar is in the vicinity of [said] a respective corner.

13. (Amended) A lead frame for an integrated circuit chip having a frame-engaging bottom surface, comprising:

a plurality of sidebars, each of said sidebars having an inner side and an outer side, said sidebars defining an aperture, said frame being sized to be accommodated entirely within corresponding outer edges of the [side] circuit chip, each side bar having an upper chip-supporting surface for engaging the [lower] bottom surface of the chip.

14. (Amended) A lead frame for an integrated circuit chip having a frame engaging bottom surface comprising:

an apertured frame said frame being generally circular and defining a [circumferential] peripheral edge and having a contact surface for securing the chip thereto, said [frame] edge being disposed within [the] an outer chip edge for minimizing fillet formation.

Approved
6-27-01
LC

FIG. 1

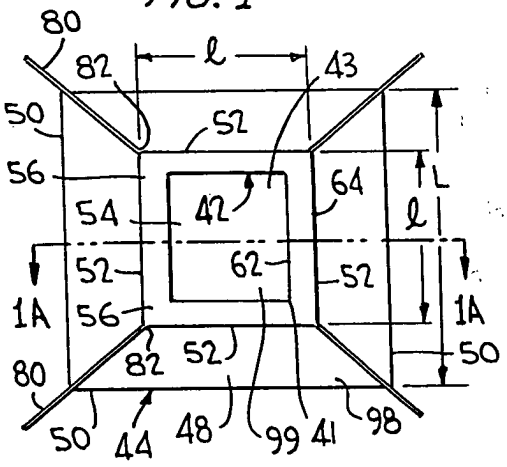


FIG. 2

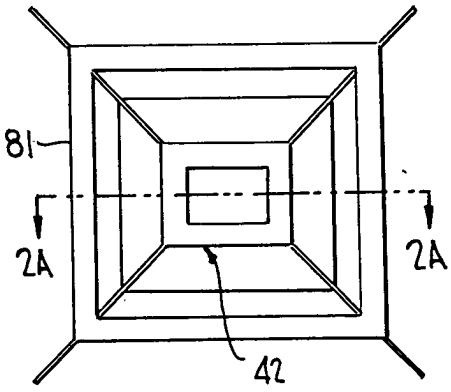


FIG. 1A

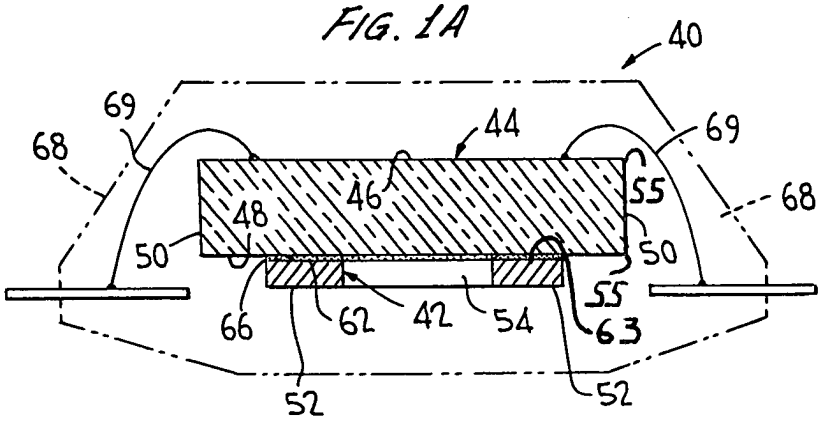


FIG. 2A

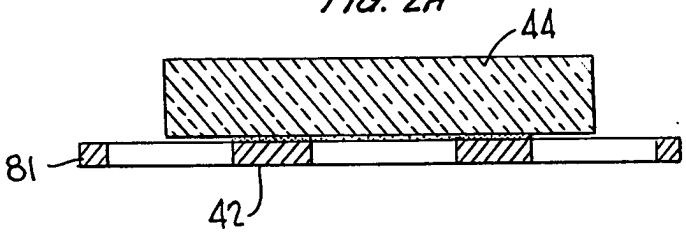


FIG. 3

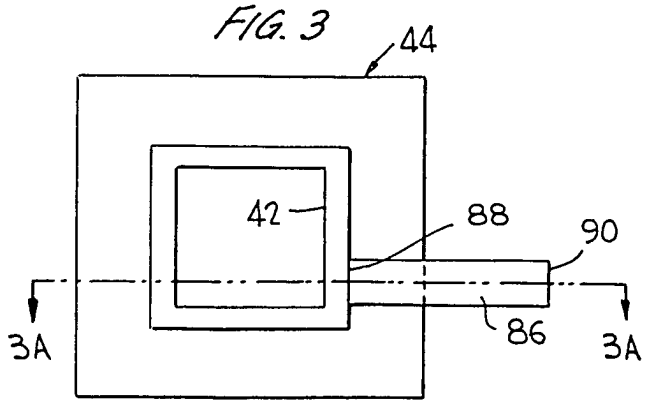


FIG. 3A

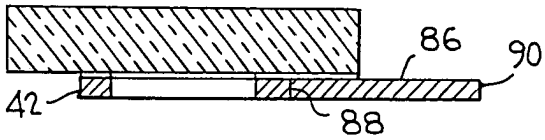
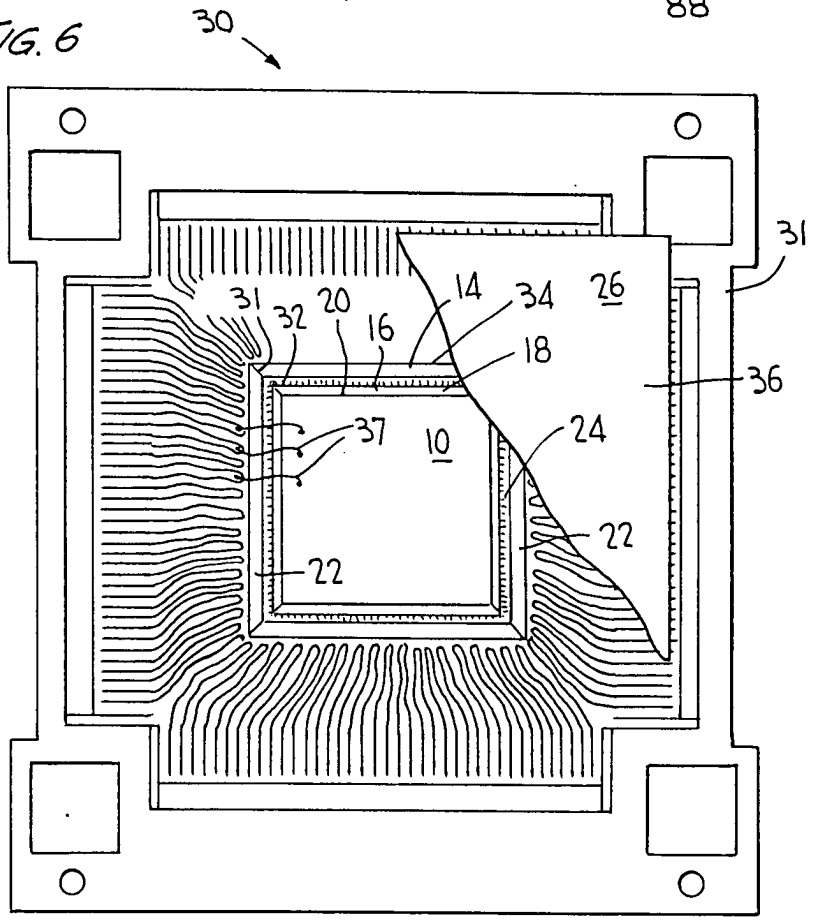


FIG. 6



PRIOR ART

FIG. 6A PRIOR ART

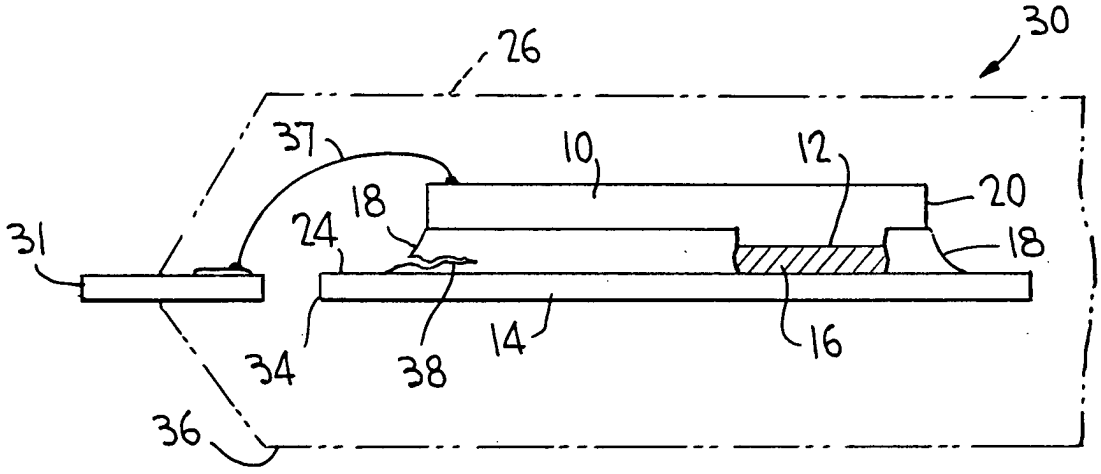


FIG. 6B PRIOR ART